IN THE CLAIMS

1. (Currently amended) A method for fabricating a semiconductor device comprising:

~~preparing a substrate having a first contact pad and a second contact pad;~~

forming a first insulating film on a substrate, the first insulating film having a first contact pad and a second contact pad;

forming a ~~first~~ second insulating film on the ~~substrate~~ first insulating film;

etching the ~~first~~ second insulating film to form a groove-shaped bit line pattern and a contact exposing the first contact pad and the second contact pad, respectively;

simultaneously forming a contact plug and a bit line in the contact and in the bit line pattern, respectively, wherein the contact plug and the ~~bitline~~ bit line have upper surfaces that are co-planar; and

forming a bottom electrode of a capacitor, the bottom electrode connected to the first contact pad.

2. (Currently amended) The method according to claim 1, wherein etching the ~~first~~ second insulating film to form a groove-shaped bit line pattern and a contact comprises:

forming a mask layer on the ~~first~~ second insulating film including the contact to expose a portion of the ~~first~~ second insulating film corresponding to the second contact pad; and

forming the bit line pattern by etching the exposed portion of the ~~first~~ second insulating film using the mask layer.

3. (Currently amended) The method according to claim 2, wherein forming the mask layer on the ~~first~~ second insulating film comprises forming a photosensitive film on the ~~first~~ second insulating film.

4. (Currently amended) The method according to claim 1, wherein etching the ~~first~~ second insulating film comprises slope-etching the ~~first~~ second insulating film.

5. (Currently amended) The method according to claim 1, wherein simultaneously forming the contact plug and the bit line comprises:

depositing a metal film on the ~~substrate~~ second insulating film including the bit line pattern and the contact; and performing a chemical mechanical polishing process.

6. (Currently amended) ~~The method according to claim 1, wherein forming the bottom electrode of the capacitor comprises:~~ A method for fabricating a semiconductor device comprising:

preparing a substrate having a first contact pad and a second contact pad;

forming a first insulating film on the substrate;

etching the first insulating film to form a groove-shaped bit line pattern and a contact exposing the first contact pad and the second contact pad, respectively;

simultaneously forming a contact plug and a bit line in the contact and in the bit line pattern, respectively, wherein the contact plug and the bit line have upper surfaces that are co-planar; and

forming a bottom electrode of a capacitor, the bottom electrode connected to the first contact pad, wherein forming the bottom electrode of the capacitor comprises, sequentially forming a second insulating film and a third insulating film on the ~~substrate~~ first insulating film~~;~~, etching the second and third insulating films to form a first opening that exposes the contact plug~~;~~, removing the contact plug to form a second opening that exposes the contact~~;~~, forming the bottom electrode in the first and second openings,~~;~~ and removing the third insulating film.

7. (Original) The method according to claim 6, wherein removing the contact plug comprises removing the contact plug with a wet etching process.

8. (Currently amended) The method according to claim 6, wherein sequentially forming the second insulating film and the third insulating film on the ~~substrate~~ first insulating film comprises:

sequentially forming an etching stopper and a sacrificial oxide film.

9. (Currently amended) The method according to claim 1, wherein forming the bottom electrode of the capacitor comprises:

forming a ~~second~~ third insulating film on the ~~substrate~~ second insulating film;

forming an opening exposing the contact plug by etching the ~~second~~ third insulating film; and forming the bottom electrode on the ~~second~~ third insulating film and inside the opening.

10. (Currently amended) The method according to claim 9, wherein the ~~second~~ third insulating film comprises:

an insulating film chosen from the group consisting of an etching stopper, an interlayer insulating film, and a stacked film of an etching stopper and an interlayer insulating film.

11. (Currently amended) A method of fabricating a semiconductor device comprising:

forming a first insulating film having a storage node contact pad and a ~~bitline~~ bit line contact pad on a ~~semiconductor~~ substrate;

forming a second insulating film having a bit line contact that exposes the ~~bitline~~ bit line contact pad on the first insulating film;

forming a ~~bitline~~ bit line contact plug in the bit line contact;

forming a third insulating film on the ~~substrate~~ second insulating film;

etching the second and third insulating films to form a groove-shaped bit line pattern and a storage node contact;

simultaneously forming a bit line and a storage node contact plug in the bit line pattern and the storage node contact, respectively, the ~~bitline~~ bit line and the storage node contact plug having upper surfaces that are coplanar;

forming a fourth insulating film and a fifth insulating film on the ~~semiconductor substrate~~ third insulating film;

etching the fourth insulating film and the fifth insulating film to form an opening that exposes the storage node contact plug;

removing the storage node contact plug to expose the storage node contact;

in the opening and the storage node contact, forming a storage node in contact with the storage node contact pad; and

removing the fifth insulating film.

12. (Currently amended) The method according to claim 11, wherein etching the second and third insulating films to form a groove-shaped bit line pattern and a storage node contact comprises:

etching the second and third insulating films to expose the storage node contact pad;

forming a mask layer on the third insulating film including the storage node contact to expose a portion of the third insulating film corresponding to the ~~bitline~~ bit line contact pad; and

forming the bit line pattern exposing the ~~bitline~~ bit line contact plug by etching the exposed portion of the third insulating film using the mask layer.

13. (Original) The method according to claim 12, wherein the first, the second, and the third insulating films are interlayer insulating films, the fourth insulating film is an etching stopper having an etching selectivity with respect to the second insulating film, the third insulating film, and the fifth insulating film, and the fifth insulating film is a sacrificial oxide film.

14. (Currently amended) A method for fabricating a semiconductor device, comprising:

forming a first insulating film having a storage node contact pad and a ~~bitline~~ bit line contact pad on a ~~semiconductor~~ substrate;

forming a second insulating film having a bit line contact that exposes the ~~bitline~~ bit line contact pad on the first insulating film;

forming a ~~bitline~~ bit line contact plug in the bit line contact;

forming a third insulating film on the ~~substrate~~ second insulating film;

etching the second and third insulating films to form a groove-shaped bit line pattern and a storage node contact;

simultaneously forming a bit line and a contact plug in the ~~bitline~~ bit line pattern and the storage node contact, respectively, the bit line and the contact plug having upper surfaces that are coplanar;

forming a fourth insulating film having an opening that exposes the contact plug on the ~~semiconductor~~ ~~substrate~~ third insulating film; and

forming a metal electrode in contact with the contact plug through the opening on the fourth insulating film.

15. (Currently amended) The method according to claim 14, wherein etching the second and third insulating films to form a groove-shaped bit line pattern and a storage node contact comprises:

etching the second and third insulating films to expose the storage node contact pad;

forming a mask layer on the third insulating film including the storage node contact to expose a portion of the third insulating film corresponding to the ~~bitline~~ bit line contact pad; and

forming the bit line pattern exposing the ~~bitline~~ bit line contact plug by etching the exposed portion of the third insulating film using the mask layer.

16. (Original) The method according to claim 14, wherein the fourth insulating film comprises a film chosen from the group consisting of an etching stopper, an interlayer insulating film, and a stacked film of an etching stopper and an interlayer insulating film.

17. (Currently amended) A semiconductor device, comprising:

a ~~semiconductor substrate~~ first insulating film having a ~~bitline~~ bit line contact pad and a storage node contact pad;

a ~~first~~ second insulating film including a groove-shaped bit line pattern that exposes the ~~bitline~~ bit line contact pad and a storage node contact that exposes the storage node contact pad, the ~~bitline~~ bit line pattern and the storage node contact having upper portions that are coplanar;

a bit line formed in the bit line pattern;

a ~~second~~ third insulating film having an opening that exposes the storage node contact; and

a bottom electrode for a capacitor formed in the storage node contact and in contact with the storage node contact pad.

18. (Currently amended) The semiconductor device according to claim 17, wherein the ~~second~~ third insulating film comprises a material having an etching selectivity with respect to the ~~first~~ second insulating film.

19. (Currently amended) A semiconductor device comprising:

a ~~semiconductor substrate~~ first insulating film having a ~~bitline~~ bit line contact pad and a storage node contact pad;

a ~~first~~ second insulating film including a groove-shaped bit line pattern exposing the ~~bitline~~ bit line contact pad and a storage node contact exposing the storage node contact pad, the ~~bitline~~ bit line pattern and the storage node contact having upper portions that are coplanar;

a bit line formed in the bit line pattern;

a contact plug formed in the storage node contact;

a ~~second~~ third insulating film having an opening that exposes the contact plug; and

a bottom electrode for a capacitor formed in the opening and in contact with the contact plug.

20. (Currently amended) The semiconductor device according to claim 19, wherein the ~~second~~ third insulating film comprises a film chosen from the group consisting of an etching stopper, an interlayer insulating film, and a stacked film of an etching stopper and an interlayer insulating film.

21. (New) The method according to claim 1, wherein forming the bottom electrode of the capacitor comprises:

sequentially forming a third insulating film and a fourth insulating film on the second insulating film;

etching the third and fourth insulating films to form a first opening that exposes the contact plug;

removing the contact plug to form a second opening that exposes the contact;

forming the bottom electrode in the first and second openings; and

removing the third fourth insulating film.

22. (New) The method according to claim 21, wherein removing the contact plug comprises removing the contact plug with a wet etching process.

23. (New) The method according to claim 21, wherein sequentially forming the third insulating film and the fourth insulating film on the second insulating film comprises:

sequentially forming an etching stopper and a sacrificial oxide film.